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Please find below and/or attached an Office communication concerning this application or proceeding.

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Continuation of 11: NOTE:

Applicant argues that the combination of Slavenburg and Martonosi does not a multi-issue processor having a first set of issue slots with holdable registers on multiple data output paths of input routing networks, and a second set of issue slots with holdable registers on a single data input path of the input routing networks.

However, as put forth in the rejections, Slavenburg teaches the register file 403 of a VLIW processor with multiple issue slots, ISSUE 1-3 (figure 3) where the processor has less issue slots than there are functional units in the machine. As an example, for a machine with 7 functional units, 3 issue slots may suffice. In general, the number of issue slots for a given number and type of functional units is a tradeoff between average performance and cost (column 3, lines 49-56) and switching matrix 401, controlled by the input switch control 902, determines which read port (input path) to connect to the inputs of which functional unit (output paths) (column 4, lines 1-3 and figure 3). Thus, as illustrated in figure 3 of the Slavenburg reference, is provided a switching matrix between the register file and the functional units used by the issue slots, to provide data from the register file 403 to the functional units. Martonosi teaches input latches 30, 32, 34 and 36, for input operands A and B sit at the inputs to the functional unit 40 holding the operands from the registers (received via lines 60 and 62) (column 4, lines 30-38 and figure 1), thus providing latches (i.e., holdable registers) to hold the operand data output from the register file to the functional units. Furthermore, it would have been obvious to one of ordinary skill in the art to use the latches holding data between the register file and the functional units, taught by Martonosi, in the VLIW processor using a switching matrix to route operand data from the register file to the individual functional units, as taught by Slavenburg, to reduce the power used in the microprocessor by detecting and disabling a predetermined number of bits that are not required for execution in the functional unit, using the operands within the input latches (Martonosi, column 4, lines 39-54).

Applicant further aruges that neither reference teaches or suggests placing the latches taught by Martonosi between the register file and switcing matrix taught by Slavenburg.

However, as the latches (i.e., holdable registers) of Martonosi hold the data being sent from the register file to the functional units, it would be purely a matter of design choice to determine whether the latches are to be placed before the switching matrix, or after it, as in either case the latches are between the register file and functional unit, holding the data sent from the register file to the functional units, and thus the operation of the system required by the claims is the same, and the latches would serve--in the same way, in both instances--to reduce the power used in the microprocessor by detecting and disabling a predetermined number of bits that are not required for execution in the functional unit, using the operands within the input latches (Martonosi, column 4, lines 39-54). Therefore the combination of Martonosi and Slavenburg used in the rejections provides a set of issue slots, including a number of functional units connected to a register file by a switching matrix, where latches (i.e., holdable registers) are placed at the input to the switching matrix in a first set of issue slots, while in a second set of issue slots they are placed at the output of the switching matrix (i.e., the input of certain functional units, in those issue slots), in both cases to reduce the power used in the microprocessor by detecting and disabling a predetermined number of bits that are not required for execution in the functional unit, using the operands within the input latches.

/Eddie P Chan/
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